

Attorney's Docket No.: 07977-088002/US3155D1

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.


Kindly include the amendments prior to initial examination of this RCE case. The claims are amended to define the subject matter.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 10/31/02



Scott C. Harris
Reg. No. 32,030

PTO Customer No. 20985



Fish & Richardson P.C.
4350 La Jolla Village Drive, Suite 500
San Diego, California 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

10225982.doc

Attorney's Docket No.: 07977-088002/US3155D1

VERSION TO SHOW CHANGES MADEIn the Claims:

Claims 1, 6, 10, 14, 16-19, 21, 24-26, 28, 39, and 40 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film formed on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said

Attorney's Docket No.: 07977-088002/US3155D1

portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening, wherein edges of at least said third opening are rounded off, and

wherein a thickness of the first interlayer insulating film is less than one third of total thickness of the first and second interlayer insulating films.

6. (Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over said semiconductor layer;

a gate electrode over the gate insulating film;

a first interlayer insulating film over said gate insulating layer and the gate electrode

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a

Attorney's Docket No.: 07977-088002/US3155D1

portion of said gate insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said gate insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

10. (Amended) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film;

Attorney's Docket No.: 07977-088002/US3155D1

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor and a portion of said insulating film where surrounds said first opening;

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of said semiconductor in the second opening, and

wherein a thickness of the first interlayer insulating film is less than one third of total thickness of the first and second interlayer insulating films.

14. (Amended) A semiconductor device comprising:

Attorney's Docket No.: 07977-088002/US3155D1

a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

[multi-interlayer insulating films comprising] at least [an upper] a first interlayer insulating [layer] film and a [lower] second interlayer insulating [layer] film over said insulating film and the gate electrode [, said lower insulating layer comprising the same material as said upper insulating layer];

at least one contact hole in said [multi-] first and second interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the [upper insulating layer] second interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the [lower insulating layer] first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

Attorney's Docket No.: 07977-088002/US3155D1

16. (Amended) A device according to claim 14, wherein said [lower and upper insulating layers] first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

17. (Amended) A device according to claim 14, wherein said [upper insulating layer of said multilayer] second interlayer insulating films has a dry etching rate higher than said [lower] first interlayer insulating layer.

18. (Amended) A device according to claim 14, wherein angles of the tapered section of the contact hole decrease successively from [a top] the second interlayer insulating layer toward a [bottom] first interlayer insulating layer.

19. (Amended) A semiconductor device comprising:

a semiconductor having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

Attorney's Docket No.: 07977-088002/US3155D1

[an] at least first and second interlayer insulating films [comprising a plurality of insulating layers] over [said semiconductor layer and] said insulating film and the gate electrode; and

a contact hole in said first and second interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section,

wherein edges of said second interlayer insulating film in said contact hole are rounded off,

wherein angles of the tapered section of the contact hole decrease successively from [a top] the second interlayer insulating [layer] film toward [a bottom] the first interlayer insulating [layer] film, and

wherein a thickness of the [bottom] first interlayer insulating film is less than one third of total thickness of the first and second interlayer insulating films.

21. (Amended) A device according to claim 19 wherein at least one of [said plurality of insulating layers in said interlayer insulating layer] first and second interlayer insulating film comprises a material selected from the group consisting of silicon nitride and organic resin.

Attorney's Docket No.: 07977-088002/US3155D1

24. (Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

[an] at least first and second interlayer insulating films [comprising a plurality of insulating layers over said semiconductor layer and] over said insulating film and the gate electrode; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of said interlayer insulating film in said contact hole are rounded off.

25. (Amended) A device according to claim 24, wherein a taper angle β of an inner surface of [an upper] the second interlayer

Attorney's Docket No.: 07977-088002/US3155D1

insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of [an lower] first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

26. (Amended) A device according to claim 24, wherein angles of the taper shape of the contact hole decrease successively from [a top interlayer insulating layer] the second interlayer insulating film toward [a bottom interlayer insulating layer] the first interlayer insulating film.

28. (Amended) A device according to claim 24 wherein at least one of [said plurality of insulating layers in said interlayer insulating layer] first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

39. (Amended) A device according to claim 14, wherein a thickness of the [lower] first interlayer insulating film is less than one third of total thickness of the [multi-] first and second interlayer insulating films.

Attorney's Docket No.: 07977-088002/US3155D1

40. (Amended) A device according to claim 24, wherein a thickness of [a lower] the first interlayer insulating film is less than one third of total thickness of the first and second interlayer insulating films.